CLASSIC CHIP

CC3M28080E

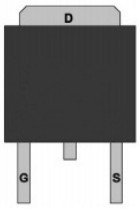
800V G2 Silicon Carbide Power MOSFET

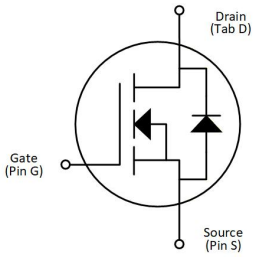
N-Channel Enhancement Mode

V_{DS}	=	800V
$R_{DS(ON)}$	=	280mΩ
$I_{D(MAX)@25^{\circ}C}$	=	12.4A

Features

- High blocking voltage with low on-resistance
- High speed switching with low capacitances
- Very low switching losses
- Avalanche ruggedness
- Temperature independent turn-off switching losses
- Integrated lumped gate resistance
- Robust against parasitic turn-on even at 0V turn-off gate voltage





Benefits

- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- PD Charger
- High voltage DC/DC converters
- Switch mode power supplies
- EV battery chargers
- PV inverters

Part number	Package Type
CC3M28080E	TO-252-3L

Maximum Ratings (T_C=25˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions
V_{DSmax}	Drain - Source Voltage	800	V	V_{GS} = 0V, I_D = 100μA
V_{GSmax}	Gate - Source Voltage	-10 /+22	V	Absolute maximum values
V_{GSop}	Gate - Source Voltage	-5 /+18	V	Recommended operational values
I_D	Continuous Drain Current	12.4	A	V_{GS} = 18V, T_C = 25˚C
		8.7		V_{GS} = 18V, T_C = 100˚C
$I_{D(pluse)}$	Pulsed Drain Current	24	A	Pulse width t_P limited by $T_{j,max}$
P_D	Power Dissipation	56	W	T_C = 25˚C, T_J = 175˚C
T_J, T_{stg}	Operating Junction and Storage Temperature	-55 to +175	˚C	/
T_L	Soldering Temperature	260	˚C	1.6mm (0.063”) from case for 10s

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	800	-	-	V	V_{GS} = 0V, I_D = 100μA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	3.0	4.0	V	V_{DS} = V_{GS}, I_D = 2mA
		-	2.1	-		V_{DS} = V_{GS}, I_D = 2mA T_J = 175˚C
I_{DSS}	Zero Gate Voltage Drain Current	-	1	10	μA	V_{DS} = 800V, V_{GS} = 0V
I_{GSS}	Gate-Source Leakage Current	-	-	200	nA	V_{GS} = 22V, V_{DS} = 0V
		-200	-	-	nA	V_{GS} = -10V, V_{DS} = 0V
$R_{DS(on)}$	Drain-Source On-State Resistance	-	280	350	mΩ	V_{GS} = 18V, I_D = 5A
		-	330	-		V_{GS} = 18V, I_D = 5A T_J = 175˚C
g_{fs}	Transconductance	-	15	-	S	V_{DS} = 20V, I_D = 5A
		-	-	-		V_{DS} = 20V, I_D = 5A T_J = 175˚C
C_{iss}	Input Capacitance	-	254	-	pF	V_{DS} = 400V V_{GS} = 0V f = 1MHz, V_{AC}=25mV
C_{oss}	Output Capacitance	-	20	-		
C_{rss}	Reverse Transfer Capacitance	-	2.5	-		
E_{oss}	C_{oss} Stored Energy	-	3.5	-	μJ	
E_{ON}	Turn-On Switching Energy	-	20	-	μJ	V_{DS} = 400V V_{GS} = -5/+18V, I_D = 5A R_G = 2.5Ω
E_{OFF}	Turn-Off Switching Energy	-	5	-		
$t_{d(on)}$	Turn-On Delay Time	-	3	-	ns	
t_r	Rise Time	-	6	-		
$t_{d(off)}$	Turn-Off Delay Time	-	5	-		
t_f	Fall Time	-	12	-		
$R_{g(int)}$	Internal Gate Resistance	-	12	-	Ω	V_{AC}=25mV, f = 1MHz
Q_{gs}	Gate to Source Charge	-	3	-	nC	V_{DS} = 400V V_{GS} = -5/+18V, I_D = 5A
Q_{gd}	Gate to Drain Charge	-	5	-		
Q_g	Total Gate Charge	-	12	-		

Reverse Diode Characteristics (T_C = 25˚C unless otherwise specified)

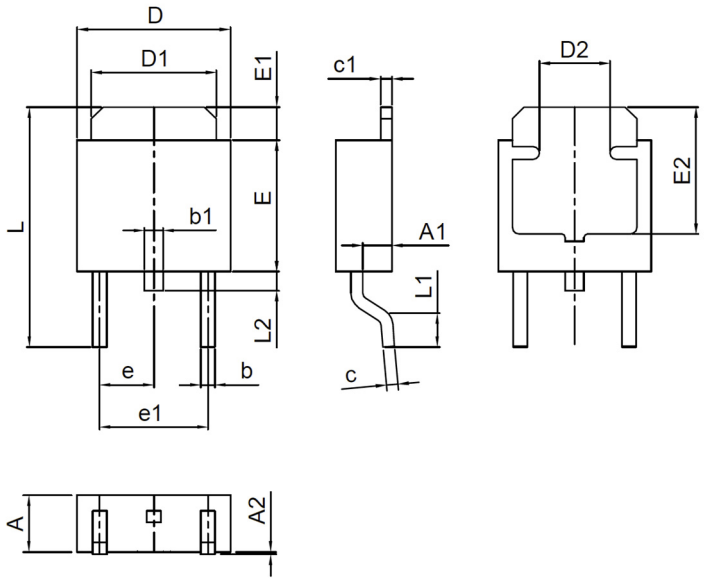
Symbol	Parameter	Typ.	Max.	Unit	Test Conditions
V_{SD}	Diode Forward Voltage	4.0	-	V	V_{GS} = -5V, I_{SD} = 2.5A
		3.7	-		V_{GS} = -5V, I_{SD} = 2.5A T_J = 175˚C
I_{SD}	Continuous Diode Forward Current	-	12	A	V_{GS} = -5V
		-	6		V_{GS} = -5V, T_C = 100˚C
t_{rr}	Reverse Recover Time	10	-	ns	V_{DD} = 400V, V_{GS} = -5V I_{SD} = 5A di/dt = 1000A/μs
Q_{rr}	Reverse Recovery Charge	54	-	nC	
I_{rrm}	Peak Reverse Recovery Current	4	-	A	

Thermal/Package Characteristics

Symbol	Parameter	Typ.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.7	˚C/W

Package Dimensions

TO-252-3L Package Outline



Dim	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	2.20	2.50	0.087	0.094
A1	1.00	1.40	0.039	0.055
A2	0.00	0.15	0.000	0.006
b	0.50	0.70	0.020	0.028
b1	0.70	0.90	0.028	0.035
c	0.40	0.60	0.016	0.024
c1	0.40	0.60	0.016	0.024
D	6.20	6.70	0.244	0.264
D1	5.10	5.50	0.201	0.217
D2	2.70	3.20	0.106	0.126
E	5.20	5.80	0.205	0.228
E1	1.20	1.60	0.047	0.063
E2	5.00	5.60	0.197	0.220
e	2.20	2.40	0.087	0.094
e1	4.40	4.80	0.173	0.189
L	9.70	10.40	0.382	0.409
L1	1.40	1.70	0.055	0.063
L2	0.60	1.20	0.024	0.047

Revision History

Document Version	Date of Release	Brief Summary
Rev.0.1	2026-04-25	Draft.

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